CDA 4203L Sec 001

Computer System Design Lab

Lab 3 Report

Programmable BCD Counter

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| --- | --- |
| Today’s Date: |  |
| Team Members: |  |
|  |
|  |
| Work Distribution: | Briefly explain the tasks completed by each team member |
| No. of Hours Spent: |  |
| Exercise Difficulty:  (Easy, Average, Hard) |  |
| Any Other Feedback: |  |

**Problem 1:** Draw overall block diagram of the programmable counter. Briefly explain how your design works. For each block, include the Verilog code (adequately comment your code). *Use as many pages as needed.*

**Problem 2:** Testbench code: Include your Verilog testbench. *Use as many pages as needed.*

**Problem 2:** Simulation Waveforms. Include waveforms that demonstrate the functionality. *Use as many pages as needed.*

**Problem 3:** Include the **.ucf** file.